

EXHIBIT Q

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.,)	
)	
Plaintiff,)	
)	
vs.)	Civil Action No. 2:21-CV-463-JRG
)	
SAMSUNG ELECTRONICS CO., LTD.,)	JURY TRIAL DEMANDED
SAMSUNG ELECTRONICS AMERICA,)	
INC., SAMSUNG SEMICONDUCTOR,)	
INC.,)	
)	
Defendants.)	

**PLAINTIFF NETLIST, INC.'S REPLY IN SUPPORT OF OPENING CLAIM
CONSTRUCTION BRIEF**

TABLE OF CONTENTS

	<u>Page</u>
I. Power-Management Integrated Circuit (“PMIC”) Patents (’918 and ’054 Patents).....	1
A. Regulated Voltage Limitations: Defendants’ Brief, II.A.3, 4	1
B. “dual buck converter”: Defendants’ Brief, II.A.1	2
C. “a second plurality of address and control signals”: Defendants’ Brief, II.A.5.....	3
D. “pre-regulated input voltage”: Defendants’ Brief, II.A.2.....	3
II. High Bandwidth Memory (“HBM”) Patents (’060 and ’160 Patents)	4
A. “array die”: Defendants’ Brief, II.B.1	4
B. “chip-select signal”: Defendants’ Brief, II.B.2	5
III. ’506 Patent.....	6
A. “before receiving the input C/A signals ...”: Defendants’ Brief, II.C.1.....	6
IV. ’339 Patent.....	6
A. The “drive” Terms: Defendants’ Brief, II.D.1	6
B. The “module controller” Terms: Defendants’ Brief, II.D.2	9
C. “latency parameter”: Defendants’ Brief, II.D.3	10

TABLE OF AUTHORITIES

Page(s)

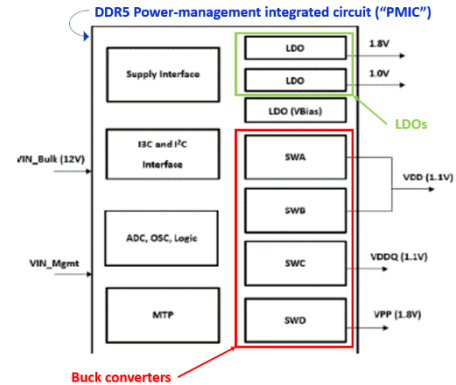
Cases

<i>Estech Systems v. Target Corp.</i> , 2021 WL 1090747 (E.D. Tex. Mar. 21, 2021)	2
<i>Hill-Rom Servs., Inc. v. Stryker Corp.</i> , 755 F.3d 1367 (Fed. Cir. 2014).....	9

I. Power-Management Integrated Circuit (“PMIC”) Patents (’918 and ’054 Patents)

A. Regulated Voltage Limitations: Defendants’ Brief, II.A.3, 4

Samsung’s refusal to explain what it seeks to import via the term “distinct” appears to be a litigation tactic. The figure at right depicts multiple buck converters (red box). SWA, SWB, and SWC each have a regulated output voltage of 1.1V. Even though they have physically distinct output voltages, Samsung apparently intends to argue that the fact that their target numerical value is the same means that each output voltage from each separate buck converter (i.e. SWA, SWB, and SWC) is not distinct. Whether the numerical value of each regulated output voltages are the same or different is irrelevant. There are still an enumerated number of regulated outputs in the device. Any assertion that the regulated voltages must be **numerically** different is contradicted by Samsung’s admission that distinctiveness of the voltage does not hinge on whether voltage amplitudes are different. Samsung asserts that dependent claim limitations specifically requiring one voltage amplitude to be less than the other “serve[] only to limit *how* those two amplitudes must be distinct.” Dkt. 82 at 9. According to Samsung then, two voltages may be “separate” even if they have the same amplitude. *See* Ex. 30 (’918 Pet.) at 30 (“[A]lthough V_{DD} and V_{DDQ} and V_{DDL} are all 1.8V, they are expressly identified as **separate** voltages....”). This must mean that “distinct[ness]” of voltage – whatever Samsung imagines that means – has nothing to do with the **value** of the voltage.



Samsung then alleges that the specification teaches “components requiring the same voltage receive a single voltage from a single output, and components requiring different voltages receive them from different voltage outputs.” Dkt. 82 at 9. But this is just an example. Samsung concedes there is no “disavowal,” and it does not dispute that the ’918 discloses an embodiment where the 1.8V supplied to volatile memory 1032 and non-volatile memory 1042 “are powered using independent

voltages and are not both powered using the first voltage 1102.” Ex. 3, 29:39-44, 29:61-64; *contra* Dkt. 82 at 9. This embodiment describes the supply of two distinct regulated voltages. The fact that they are numerically the same does not detract from the fact that there are two separate regulated voltages.

Samsung also invokes an alleged rule that “separately-listed claim elements must be ‘distinct,’” without explaining what it means by “distinct.” Dkt. 82 at 9-10. However, the cases cited by Samsung confirm that elements delineated by “first” and “second” can still share overlapping characteristics, and rightly reject attempts by defendants import limitations from the specification. *Id.* at 7-8. *Estech Systems v. Target Corp.* is instructive. There, the defendant sought to construe “a first local area network (‘LAN’),” “a second LAN,” “a wide area network (‘WAN’),” and “a third LAN” to require that “the LANs and WAN are different.” 2021 WL 1090747, at *19 (E.D. Tex. Mar. 21, 2021). The Court rejected this construction, finding that while they are “separately recited [terms] in the claims [that] are distinct components,” that “[did] not mean ... that two LANs or a LAN and a WAN cannot be of the same type of network.” *Id.* Here, while the claims require the enumerated regulated voltages and voltage amplitudes, nothing precludes the voltage amplitudes from being the same numerical level.

B. “dual buck converter”: Defendants’ Brief, II.A.1

Samsung avoids explaining what it means by “distinct ... voltages.” Dkt. 82 at 2-4. Nor does Samsung point to any language in the patents that supposedly “define[]” “dual buck converter” as one “outputting two voltages with different voltage levels,” or contend there is any express disclaimer. *Id.*

As with the “regulated voltage” terms above, Samsung argues that the outputs of the dual buck converter 1124 in Fig. 16 must have different voltage amplitudes. *Id.* at 3. Neither the intrinsic nor extrinsic evidence supports that position. Specifically, Samsung argues that, with respect to the output voltages 1104 and 1105 of dual-buck converter 1124 depicted in Fig. 16, if voltage 1105 “is to be used by a different component of the memory system,” then it must have “a different voltage value than voltage 1104.” Dkt. 82 at 3. That is incorrect. In the cited embodiment, voltage 1104 is 2.5V for

powering an isolation switch and voltage 1105 “is used to power the controller 1062 (e.g. FPGA).” *Id.* (citing 29:46-50). But FPGAs were designed to operate at different operating voltages: some at 1.2V, some at 2.5V and some at yet other voltages. *See* Ex. 29 at 2 (table excerpt below, with each column listing operating voltages for a different FPGA ranging from 1.0V to 2.5V). In other words, there is nothing that requires different components on the memory module to operate at different voltages.¹

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V _{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A

The claim language is clear: two buck converters are “configured to operate as a dual buck converter,” not “combine[d] ... to output two distinct regulated voltages.” Ex. 3, cl. 2; *contra* Dkt. 82 at 2.

C. “a second plurality of address and control signals”: Defendants’ Brief, II.A.5

Samsung does not dispute that the claims already distinguish the “second” plurality of the C/A signals as the output of the first circuit, in contrast to the “first” plurality that is input to the first circuit. *See* Dkt. 76 at 22-23. Samsung does not explain what its proposed construction adds, other than confusion about the meaning of the word “distinct.” Dkt. 82 at 11-12. Nor does Samsung point to any evidence that bars the output signals from being the same value as the input.

D. “pre-regulated input voltage”: Defendants’ Brief, II.A.2

The “pre-regulated input voltage” is an input to a buck converter and the claimed “input voltage” is one received from the module’s “edge connections.” Dkt. 76 at 25-26. The memory module need not use the received input voltage to generate the pre-regulated input voltage on module. For example, the ’918 specification describes power element 1140 (including the capacitor array 1142) as the “source[]” of the pre-regulated input voltage 1112. Ex. 3, 28:53-58. Voltage 1112 is a pre-regulated input voltage used “in the third state,” when it is detected that “the trigger condition [such as power

¹ *See also*, Ex. 3 (’918), 29:39-44 (same voltage 1102 used to operate memories and FPGA); Ex. 30 (’918 Pet.) at 86 (Samsung showing V_{DD} for DDR2 and V_{CCFPGA} for FPGA can **both be set** at 1.8V).

failure] has occurred.” *Id.*, 28:39-58. That is, voltage 1112 is used when the input voltage 1106 from the edge connections is not available. Thus, contrary to Samsung’s assertion, voltage 1112 is not generated using the input voltage 1102 received at the edge connections, but from power supply 1140.

Samsung denies the linkage between Figures 12 and 16. But the “third” state in Figure 16 for which power supply 1140 and voltage 1112 are used corresponds to the “second” state in Figure 12 for which “a second power supply 1080” is used. *Id.*, 25:54-62. Like 1140, power supply 1080’s capacitor can be charged by the system voltage when it is present and used when power failure occurs. *Id.*, 26:8-30. The ’918 further links Figures 12 and 16 by noting that the memory module of Figure 16 can include “the second power supply 1080 and the switch 1090.” 27:65-28:2. Hence, power element 1140 is an example of 1080. The specification teaches that 1080 can be, but need not be, on the same module board 1020 as the memory system. *Id.*, 26:26-35. As such, element 1140, which generates the pre-regulated input voltage 1112, need not be on the same module board as the memory system. Samsung’s insistence for on-module regulation of input voltage to buck converter is not supported.

II. High Bandwidth Memory (“HBM”) Patents (’060 and ’160 Patents)

A. “array die”: Defendants’ Brief, II.B.1

Samsung does not dispute that “array dies” refers to dies including memory cells. Dkt. 76 at 27. Samsung argues Netlist disclaimed “DRAM circuits.” Dkt. 82 at 13-16. This contradicts Samsung’s admission before the PTO that there was no such disclaimer. Samsung’s IPRs map the claimed “array dies” squarely on disclosures involving DRAM circuits. Ex. 31 at 39-40 (Kim’s “slave chips,” “DRAM internals” figure). Moreover, Netlist’s statement only concerned Rajan’s stacked “DRAM circuits 206A-D,” and only as a prelude for the explanation as to why Rajan’s buffer die does not disclose the “control die.” Ex. 26 at 10 (stating that “[a]s a result” of Rajan’s stacked DRAM circuits 206A-D not being array dies, Rajan’s buffer die does not disclose the required elements of a claimed “control die”).

A POSITA reading the prosecution history as a whole would not understand that Netlist had

disclaimed DRAM circuits. Netlist explained that the same arguments for distinguishing Rajan from claim 1 were “applicable to claim 29” that recites a “**DRAM package**” comprising “a plurality of array dies arranged in a stack” and other features of the memory package of claim 1. Dkt. 76 at 27-29; Ex. 26 at 10, 14. Samsung does not dispute that “array dies” in the two claims should be accorded the same meaning. Dkt. 82 at 15. Rather, Samsung misdirects by contending Netlist has not shown “how claim 29’s reference to a ‘DRAM package’ means that array dies are *identical* with DRAM circuits.” *Id.* at 20. But to the extent that Samsung’s construction excludes any DRAM circuit or cells from the construction of “array dies,” it does not explain how a “DRAM package” of claim 29 can comprise a stack of “array dies” having only non-DRAM cells and still be called a “DRAM package.” It also does not explain what it means by “array die that is different from a DRAM circuit.” For instance, which DRAM circuit must the “array dies” be different from, *e.g.*, even ones that are specifically described in the patent, or only Rajan’s DRAM circuits 206A-D? Samsung does not explain how much of a difference its construction contemplates. For example, Samsung admits that HBM products “differ[] from the DDR4 or DDR5 DIMM[s]” (Dkt. 26 at 7-8), but there may be some similarity in how DRAM cells are constructed. The fact that Samsung’s construction does not even match the alleged disclaimer, “Rajan’s DRAM circuits 206A-D,” and that it does not explain the relationship between these specific circuits and its generic language “DRAM circuits” show that its disclaimer argument lacks merit.

B. “chip-select signal”: Defendants’ Brief, II.B.2

The specification supports the inclusion of “enabling” in Netlist’s construction. Ex. 5, 1:49-56 (“chip select signals to enable or select the array dies for data transfer”). Further, “one or more” is consistent with the load-reduction goal of the invention because load reduction results from having die interconnects be in electrical communications with some but not all array dies; and that is a feature recited by the “die interconnect” elements of the claims. *E.g.*, Ex. 5, cl.1, 2:8-15, 7:9-8:18, 11:6-12:16.

III. '506 Patent

A. “before receiving the input C/A signals ...”: Defendants’ Brief, II.C.1

Pointing to amendments pertaining to “before the memory read operation” (“Amended Term”), Samsung insists that “before receiving the input C/A signals corresponding to the memory read operation” (“Before Step”) must mean “during one or more previous operations.” Dkt. 82 at 18-20. Samsung’s logic is flawed. **First**, Netlist’s decision to not extend the amendment to the Before Step should be respected. Indeed, the differential treatment of the Amended Term and the Before Step confirms that the inventors did not intend the Before Step to mean “during one or more previous operations.” **Second**, Samsung’s argument that “‘receiving the input C/A signals corresponding to the memory read operation’ is the *first* step of a memory read operation” is factually incorrect. Dkt. 82 at 19. Prior to that, there are steps such as sending corresponding C/A signals by the host, receiving the signals at the edge connections, and forwarding the signals to the module control device. Ex. 2, 3:29-40. As such, the Before Step need not occur “before the memory read operation” as Samsung assumes; and the two are not coextensive. Samsung’s construction should thus be rejected.

IV. '339 Patent

A. The “drive” Terms: Defendants’ Brief, II.D.1

Samsung proposes to read a “Fork-in-the-Road” configuration into the term “to actively drive” write data across a data buffer. Dkt. 82 at 20-26. That is simply claim redrafting. The claim language mentions neither “activat[ing]” nor “disabl[ing]” a data path, or the other 41 words that Samsung is importing. In fact, with respect to the data path, the claim provides all that is required: “the byte-wise data path is **enabled** for a first time period” Dkt. 82 at 20-26.

To the extent that Samsung suggests that Netlist disclaimed claim scope, Samsung is mistaken. Dkt. 82 at 22-23. During prosecution, Netlist explained that, in Ellsberry, “[t]he data paths ... are open by default,” i.e., that the data path is enabled even in the absence of a read or write operation.

Ex. F at 17. In contrast, the '339 patent claims a configuration in which a data path in a data buffer is closed when the memory module is **not** communicating data with the memory controller. *Id.*; *see also* Ex. G at 17 (“The data paths can thus be kept disabled to isolate the memory devices from the bus interface **when the memory module is not communicating data with the memory controller.**”); Ex. H at 21 (“The data paths can thus be kept disabled to isolate the memory devices from the bus interface, or vice versa, **when the memory module is not communicating data with the memory controller.**”).² Samsung’s referenced prosecution statement therefore has nothing to do with the “Fork-in-the-Road” configuration, which concerns switching among different data paths.³ The referenced remarks relate to turning on and off the same data path(s), as do the claims. This is consistent with the switching function of the data buffer circuit described in the '339 patent: even in a “Straight Line” configuration, data transmission between a host and a memory device is selectively allowed or inhibited when the corresponding data path is enabled or disabled. *Contra* Dkt. 82 at 23.

Thus, while the specification discusses the enabling and disabling of a data path in reference to an example with two forks, the same procedure would apply were there only a single-prong fork (*e.g.*, by focusing only on memory operations associated with Y2 terminal and the related tristate buffer). Ex. 1, 16:40-44. Samsung wrongly argues that the use of a “multiplexor” in Figure 5 supports its “Fork-in-the-Road” construction. Dkt. 82 at 25. But the '339 expressly states that “the multiplexer 508 and the read buffer 509 operations may be split over two tristate buffers, one to enable the value from Y1 to the data line 518 and another to enable the value from Y2 to the data line 518.” Ex. 1, 16:40-44. In that embodiment, the read path for Y1 can be enabled/disabled independently from that for Y2, and separately from the write data paths for Y1 and Y2. In other words, the Y2 branch operates

² A data path can be idle with no data (*e.g.*, between read and write operations). *E.g.*, cl. 19 (“wherein the data paths are disabled after the first time period and before the second time period”).

³ *See* Dkt. 82 at 21 (discussing activating/disabling of data paths “**in** a write operation”); *id.* at 22 (“Data paths A and B are similarly activated and disabled **during read operations**”).

the same, with or without the Y1 branch, and vice versa – they are each in a “Straight Line.”

Finding no express words of exclusion or restriction, Samsung nevertheless alleges Netlist fabricated disclosures that do not exist in the '339 patent. Dkt. 82 at 23. Samsung has misunderstood the disclosures of the '339 patent. The annotated figures in the opening brief are renditions of the alternative embodiments already laid out with words in the specification. Ex. 1, 9:44-49 (“[E]mbodiments with less than four ranks (e.g., **one rank**, **two ranks**, ... per memory module [] may be employed.”). For instance, the '339 patent envisions an embodiment in which “each data transmission circuit 416 is connected to **one** ...

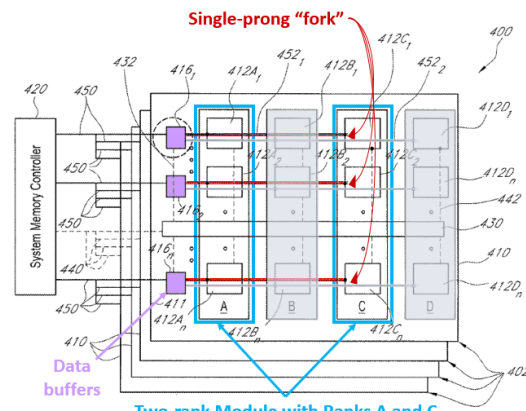


FIG. 3A

data line] 452 connected to one corresponding memory device in each of the ranks.” Ex. 1, 14:38-43. Thus, for example, instead of being connected to two data lines 452 as in the 4-rank example shown in Figure 3A, each buffer would be connected to a single data line 452 in a two-rank implementation that includes only ranks A and C (or B and D) on the memory module. *E.g.*, Ex. 1, 13:37-38, 13:58-59 (Fig. 3A/3B correspond to 4A/4B). In such a configuration, as illustrated, there is but a single-prong fork for each data buffer (highlighted in red in Fig. 3A above).

Ignoring the specification, Samsung claims the “one or more data lines” language refers only to “the number of data lines used to connect to memory devices in a particular rank,” and not “the number of data paths used to transmit data.” Dkt. 82 at 24. But as highlighted in the illustration above and in the opening brief (Dkt. 76 at 7), a single path connects a data buffer to each memory device in a single rank (*e.g.*, a single path connects 416₁ to 412A₁ and the same path connects 416₁ to 412C₁ in a different rank). To the extent Samsung complains that the inventors did not provide a specific figure for those written embodiments, the inventors are not required to repeat disclosures for every possible permutation when they operate in materially the same way.

As to load reduction, Samsung's citation to 14:59-15:4 relates to what is achieved "in certain embodiments." Dkt. 82 at 25. It does not establish that load reduction cannot be obtained in a "Straight Line." Indeed, if the host is connected to ranks A and C through a data buffer instead of directly, the host would only see a single load instead of loads corresponding to two memory ranks, as in a "Straight Line" layout. *See* Dkt. 77-1 at 10; Samsung's Tech. Tutorial, at 4; Ex. 1, 16:45-54 (cited on Dkt. 76 at 8). Samsung argues that because the claims of the '186 patent were limited to a "Fork-in-the-Road" configuration, the same must be true here. Dkt. 82 at 25-26. Nonsense. The '339 claims do not recite the "selectively isolate" or "selectively allow" language of the '186. *See* Dkt. 76 at 5 (claim comparison). As to the '907 patent, the Commission vacated the ALJ's original construction that applied the "Fork-in-the-Road" layout. The ALJ then decided that the restriction was improper; the Commission then based its fact finding on the ALJ's revised construction. Ex. 8 at 1-3; Ex. 9 at 8-13.

B. The "module controller" Terms: Defendants' Brief, II.D.2

Samsung does not dispute that the "module controller" terms place no express limit on the number of ranks the input or output signals correspond to. Samsung nevertheless seeks to add 35 words to import such a limitation. Dkt. 76 at 8-9; Dkt. 82 at 26-29. Samsung argues that the '386 claims are "irrelevant," but a comparison of the '386 claims (limited to rank multiplication) and the '339 claims indisputably show that the '339 claims do not require rank multiplication. Dkt. 76 at 10.

Samsung incorrectly claims that the '339 discloses "[n]o other examples of control circuits," citing to a single sentence referencing "**examples** of circuits." Dkt. 82 at 27 (citing 10:50-53). Even assuming Samsung is correct (it is not), the Federal Circuit is clear that claims are not to be read restrictively "[e]ven when the specification describes only a single embodiment" absent "clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371-72 (Fed. Cir. 2014). Samsung has not even attempted to make this showing. Further, in contrast to each case Samsung cites (Dkt. 82 at 29), the

specification discloses multiple examples of a “control circuit” that do not require rank multiplication. Dkt. 76 at 11 (citing Ex. 1, 10:38-41); Ex. 1, 10:21-32 (examples of “control circuit” including PLDs, ASICs, FPGAs, CPLDs with no limit on input/output signals). The specification also teaches that the circuit may function in a manner comparable to a “conventional RDIMM” (10:38-43), *e.g.*, as in the two-rank RDIMM depicted in the opening brief, which receives and outputs the *same* number of chip-select signals (two). Dkt. 76 at 11. As such, the output and input signals correspond to the same number of ranks: no rank multiplication is required. *See id.* Samsung argues that the specification “says nothing about the control signals that are output from the control circuit.” Dkt. 82 at 28. This ignores that a POSITA would understand the reference to a “conventional RDIMM” as referring to a JEDEC-standard RDIMM,⁴ which Samsung also does not dispute. Samsung is mistaken in its assertion that Netlist excludes preferred embodiments: Netlist’s proposed construction allows for, even though it does not require, rank multiplication, and thus does not exclude any preferred embodiments.

C. “latency parameter”: Defendants’ Brief, II.D.3

Samsung does not dispute that latency affects both the start and end time periods, as explained in the opening brief. Dkt. 82 at 29-30. As such, the “latency parameter” affects both the start and the duration of the claimed time periods. Dkt. 76 at 14-15. The prosecution history does not counsel otherwise. *Contra* Dkt. 82 at 30. There, Netlist explained when amending the “specific time period” language that “JEDEC Standard 21-C is about timing agreements between the *memory devices and the memory controller*,” and not about the data path enablement in data buffer. Ex. H at 20. The examiner allowed the claims, “find[ing] the amendments submitted 7/24/2020 in light of the remarks submitted therewith to overcome the prior art of record.” Ex. 32 at 2. As such, the alleged prior art does not provide the alleged plain and ordinary meaning for the term.

⁴ Samsung has conceded that a POSITA would be familiar with this standard. Ex. 33 (‘339 Pet.) at 3.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that, on September 23, 2022, a copy of the foregoing was served to all counsel of record.

/s/ Jason Sheasby
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